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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,687	07/20/2006	Ryotaro Kudo	XA-10598	7339
181 7590 04/30/2009 MILES & STOCKBRIDGE PC 1751 PINNACLE DRIVE SUITE 500 MCLEAN, VA 22102-3833				
			EXAMINER ZHANG, JUE	
			ART UNIT 2838	PAPER NUMBER
			NOTIFICATION DATE 04/30/2009	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@milestockbridge.com
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Office Action Summary

Application No.

10/586,687

Applicant(s)

KUDO ET AL.

Examiner

JUE ZHANG

Art Unit

2838

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 48-94 is/are pending in the application.
- 4a) Of the above claim(s) 48-58, 69-75 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 76-82 and 89-94 is/are allowed.
- 6) ☐ Claim(s) 59-61, 63-64, 68, 83-88 is/are rejected.
- 7) ☐ Claim(s) 62 and 65-67 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 July 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-846)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 7/20/2006; 2/12/2009
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 59-68, 76-94 reading on invention Group 2 in the reply filed on 02/12/2009 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 59-61, 63, 83-88 are rejected under 35 U.S.C. 102(b) as being anticipated by Katsuji (US Patent No. 6359493, hereinafter '493).

Claim 59, '493 teaches a voltage level shifting circuit (Fig. 1-3) comprising:

a MOSFET (e.g., 104) which has either one of source/drain routes thereof connected to an input node to which an input voltage is supplied and has a predetermined voltage supplied to a gate thereof (e.g., note 201)(col. 6, lines 66-67)(Fig. 1, 3);

a current source which is provided between another source/drain route of the MOSFET and a ground potential of the circuit and allows a DC current component to flow therethrough (e.g., the current provided by 114)(Fig. 1), wherein

the voltage level shifting circuit obtains an output voltage (e.g., the voltage at note 102 as function of/ or the voltage at note 203) from another source/drain route of the MOSFET (Fig. 1, 3).

Claim 60, '493 teaches the limitations of claim 59 as discussed above. It further teaches that wherein a capacitor (e.g., 113)(Fig. 1) is provided in parallel to the current source.

Claim 61, '493 teaches the limitations of claim 60 as discussed above. It further teaches that wherein the capacitor is a MOS capacity which is configured to have a sufficiently large capacity value with respect to a drain-source parasitic capacity of the MOSFET, and the current source is a depression type MOSFET which connects a gate and a source thereof to each other (Fig. 1 and corresponding text).

Claim 63, '493 teaches the limitations of claim 59 as discussed above. It further teaches that wherein the voltage level shifting circuit is mounted on one semiconductor substrate (Fig. 1 or 3).

Claim 83, '493 teaches a voltage level shifting circuit comprising:

an input terminal to which an input voltage is supplied;

a MOSFET (e.g., 104) which has either one of source/drain routes thereof connected to the input terminal and has a predetermined voltage supplied to a gate thereof (e.g., note 201)(col. 6, lines 66-67)(Fig. 1, 3); and

a part (e.g., 114) which is provided between another source/drain route of the MOSFET and a ground potential of the circuit (e.g., the current provided by 114)(Fig. 1), wherein

the voltage level shifting circuit obtains an output voltage (e.g., the voltage at node 102 as function of V203) from another source/drain route of the MOSFET, and when the input voltage is equal to or more than a voltage corresponding to the predetermined voltage, the output voltage corresponding to the predetermined voltage is outputted from another source/drain route (Fig. 2.), and

the part is configured such that a current which brings a voltage of another source/drain route close to the ground potential is allowed to flow in the part when a voltage larger than the ground potential is applied to another source/drain route (e.g., the signal at node 203 when the level at LOW)(Fig. 2).

Claim 84, '493 teaches the limitations of claim 83 as discussed above. It further teaches that wherein when the input voltage is less than a voltage corresponding to the predetermined potential, the output voltage corresponding to the input voltage is outputted from another source/drain route (Fig. 1-3).

Claim 85, '493 teaches the limitations of claim 83 as discussed above. It further teaches that wherein a current which brings a voltage of another source/drain route close to the ground potential is a fine current which is not considered as a defect of the voltage level shifting circuit (e.g., the current through 114 when it performing normal function as being designed)(Fig. 1-3).

Claim 86, '493 teaches the limitations of claim 83 as discussed above. It further teaches that wherein a capacitor (e.g., 113) is provided in parallel to the part (Fig. 1, 3).

Claim 87, '493 teaches the limitations of claim 83 as discussed above. It further teaches that wherein the part is a depression type MOSFET which connects a gate and a source thereof to each other (Fig. 1, 3).

Claim 88, '493 teaches the limitations of claim 83 as discussed above. It further teaches that wherein the part is a resistance element (e.g., when 114 conducting current it acting as an active resistance) formed of poly-silicon (Fig. 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1,148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuji (US Patent No. 6359493, hereinafter '493) in view of Peng et al, (US Patent No. 7276953, hereinafter '593).

Claim 64, '493 teaches the limitations of claim 63 as discussed above. It further teaches that the voltage level shifting circuit is mounted on a semiconductor integrated circuit device (i.e., as improvement of the conventional circuit used in LSI)(col. 1, line 7-23).

'493 does not explicitly disclose that the input node is an external terminal of the semiconductor integrated circuit device, and an electrostatic breakdown preventing circuit is provided thereto. However, it is known to one of ordinary skill in art, as example disclosed by '953, that a signal can be inputted or outputted by routing the signal to a designated IO terminal pin (e.g., VINHV) of the IC to provide the external accessibility of the circuit, with proper ESD protection provided (e.g., 226) in order to prevent the IC from electrostatic damage (Fig. 2). Therefore, the subject as whole would have been obvious to one of ordinary skill in art at the time of invention to have routed the input signal to an external terminal with proper ESD protection circuit in order to have provided external accessibility for the circuit, as it is known to one in art at the time of invention, as demonstrated by '953, it is a suitable method in order to provide external accessibility for a IC.

7. Claim 68 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuji (US Patent No. 6359493, hereinafter '493) in view of Kamenicky (US Patent No. 6670842, hereinafter '842).

For claim 68, '493 discloses the claimed invention except for a substrate of the MOSFET is connected to another source/drain route of the MOSFET. '842 discloses a circuit using MOSFET device. '842 further discloses that by connecting the drain and

substrate of the device together EMC can be improved. Therefore, the subject as whole would have been obvious to one of ordinary skill in art at the time of invention to have connected the drain with the substrate of the MOSFET of '493, as taught by '842, in order to have improved the EMC of the circuit, as it is known to one in art at the time of invention, as demonstrated by '842, it is a suitable method in order to improved the EMC of the circuit.

Allowable Subject Matter

8. Claims 62, 65-67 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
9. Claims 76-82, 89-94 are allowable over the prior art of record.

The following is a statement of reasons for the indication of allowable subject matter:

For claim 62, 66, the prior art does not fairly teach or suggest that the voltage level shifting circuit as claimed in claim 61, the output voltage being supplied to an input of a first CMOS inverter circuit which is operated with a power source voltage smaller than the input voltage, and the predetermined voltage is the power source voltage.

For claim 65, the prior art does not fairly teach or suggest that the voltage level shifting circuit as claimed in claim 61, further having an output signal of the first CMOS inverter circuit is transmitted to an input of a second CMOS inverter circuit on a next stage, and an output signal of the second CMOS inverter circuit is fed back to a gate of

the MOSFET which is provided between an input terminal of the second CMOS inverter circuit and a ground potential of the circuit thus allowing the first CMOS inverter circuit to possess a hysteresis transmission characteristic..

For claim 67, the prior art does not fairly teach or suggest that the voltage level shifting circuit as claimed in claim 60, further having the output voltage is supplied to an input part of an input circuit which is operated with a power source voltage smaller than the input voltage, the predetermined voltage is the power source voltage, and the input circuit includes a capacitive component in parallel to the capacitor.

For independent claim 76: No prior art uncovered anticipates or renders obvious applicant(s) claimed the limitations for a semiconductor integrated circuit device having:

- a first switching element which controls a current for forming an output voltage by dropping an input voltage;

- a terminal which allows the current to pass therethrough; a second switching element which performs a switching operation which possess time in which the second switching element assumes an ON state when the first switching element assumes an OFF state thus controlling the current;

- a first driving circuit which is operated by a first voltage corresponding to an input voltage thus driving the first switching element;

- a second driving circuit which is operated by a second voltage thus driving the second switching element; and

- a control logic circuit which is operated by the input voltage or a third voltage which is equal to or less than the second voltage, and forms a driving signal for the first

driving circuit and the second driving circuit by receiving control signals for the first switching element and the second switching element, wherein the control logic circuit includes a first voltage level shifting circuit which shifts a voltage level of a driving signal for the first switching element in response to the third voltage and feedbacks the driving signal of the first switching element to an input of the second driving circuit, and a second voltage level shifting circuit which shifts a voltage level of a driving signal for the second switching element in response to the third voltage and feedbacks the driving signal for the second switching element to an input of the first driving circuit, and performs a switching control to prevent the first and second switching elements from simultaneously assuming an ON state, and the first switching element, the terminal, the second switching element, the first driving circuit, the second driving circuit and the control logic circuit are sealed in one package.

The remaining 77-82, 89-94 are allowable for being dependent claims of the corresponding allowable independent claims.

Examiner's Note:

10. Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as

well as the context of the passage as taught by the prior art or disclosed by the Examiner.

11. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUE ZHANG whose telephone number is (571)270-1263. The examiner can normally be reached on M-Th 7:30-5:00PM EST, Other F 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm Ullah can be reached on 571-272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Akm Enayet Ullah/
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JZ